Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please cancel claims 2-5, 7, 9-12, 14-19, 21-26 and 31-34, amend claims 1, 6, 8, 13, 20, 30, and add new claims 35-49, as follows:

Listing of Claims:

1. (Currently Amended) A memory system, comprising:

a memory device having at least one extraneous device pin;

a memory controller configured to control the memory device; and

a signal path extending between the memory device and the controller that includes the at least one extraneous device pin, the signal path being operable to a transfer a selected memory system characteristic between the controller and the memory device, wherein the selected memory system characteristic further comprises time delay information operable to at least approximately center data communicated to and from the memory device within a data eye.

2.-5 (Canceled)

6. (Currently Amended) The memory system of claim ~~3~~1, wherein the time delay information is generated within the memory controller, and the memory device is configured to receive the time delay information and to apply the information to time shift data transferred by the memory device.

7. (Canceled)

8. (Currently Amended) A memory system, comprising:

a memory device having an unused device pin and a plurality of memory cells;

a memory controller configured to control the memory device;

a first signal path and a second signal path distinct from the first signal path that couple the memory device and the memory controller, wherein the first signal path includes the unused device pin, wherein the memory controller further comprises a data eye learning block operable to generate a time delay interval signal, and the data eye learning block communicates the time delay interval signal to the memory device on the first signal path.

9.-12 (Canceled)

13. (Currently Amended) The memory system of claim ~~12~~8, wherein the memory device further comprises a plurality of data lines coupled to the plurality of memory cells, and the data lines communicate data signals to the data eye learning block on the second signal path.

14.-19 (Canceled)

20. (Currently Amended) A computer system comprising:

a memory system including a memory device and a controller;

at least one extraneous pin coupled to the memory device;

a signal path coupling the memory device to the controller that includes the at least one an extraneous pin; and

a processor coupled to the memory system, wherein the memory controller further comprises a data eye learning block that receives output data from the memory device and generates a time delay value that at least approximately aligns the output data within a data eye, the time delay value being communicated to the memory device on the signal path.

21.-26 (Canceled)

27. (Original) The computer system of claim 20, wherein the controller is further coupled to address, data, and control busses that are further coupled to the processor.

28. (Original) The computer system of claim 20, further comprising at least one data storage device coupled to the processor.

29. (Original) The computer system of claim 20, further comprising at least one output device coupled to the processor.

30. (Currently Amended) The computer system of claim 20~~200~~, further comprising at least one input device coupled to the processor.

31.-34 (Canceled)

35. (New) A memory system, comprising:

a memory device having at least one extraneous device pin;

a memory controller configured to control the memory device; and

a signal path extending between the memory device and the controller that includes the at least one extraneous device pin, the signal path being operable to a transfer a selected memory system characteristic between the controller and the memory device, wherein the selected memory system characteristic further comprises parity information generated within the memory device.

36. (New) The memory system of claim 35, wherein the memory system further includes a comparator within the controller that compares a logic state of the parity information generated within the memory device with a logic state of parity information generated within the controller and generates a parity flag value based on the comparison.

37. (New) A memory system, comprising:

a memory device having an unused device pin and a plurality of memory cells;

a memory controller configured to control the memory device;

a first signal path and a second signal path distinct from the first signal path that couple the memory device and the memory controller, wherein the memory device further

comprises a plurality of data lines coupled to the plurality of memory cells and a first comparison gate coupled to the data lines, the first comparison gate being operable to successively compare a logic state on each of the plurality of data lines and to generate a first parity value based on the successive comparison, the first parity value being communicated to the controller on the first signal path.

38. (New) The memory system of claim 37, wherein the memory controller receives a plurality of data signals communicated on the second data path, and the controller further comprises a second comparison gate that receives the data signals and is operable to successively compare a logic state associated with the data signals, the second comparison gate generating a second parity value based upon the comparison.

39. (New) The memory system of claim 38, wherein the memory controller further comprises a comparator that receives the first parity value and the second parity value and compares a logic state of the first parity value to a logic state of the second parity value and generates a parity check signal based upon the comparison.

40. (New) The memory system of claim 37, wherein the first comparison gate comprises a XOR logic gate.

41. (New) The memory system of claim 38, wherein the second comparison gate comprises a XOR logic gate.

42. (New) The memory system of claim 39, wherein the comparator comprises a XNOR logic gate.

43. (New) A computer system comprising:

a memory system including a memory device and a controller;

at least one extraneous pin coupled to the memory device;

a signal path coupling the memory device to the controller that includes the at least one an extraneous pin; and

a processor coupled to the memory system, wherein the memory device further comprises a first comparison gate within the memory device that is coupled to data lines and generates a first parity value therefrom, the first parity value being communicated to the controller on the signal path.

44. (New) The computer system of claim 43, wherein the controller further comprises a second comparison gate that generates a second parity value.

45. (New) The computer system of claim 44, wherein the controller further comprises a comparator that receives the first parity value and the second parity value and generates a parity flag therefrom.

46. (New) The computer system of claim 43, wherein the controller is further coupled to address, data, and control busses that are further coupled to the processor.

47. (New) The computer system of claim 43, further comprising at least one data storage device coupled to the processor.

48. (New) The computer system of claim 43, further comprising at least one output device coupled to the processor.

49. (New) The computer system of claim 43, further comprising at least one input device coupled to the processor.